PHASE CLOCK SELECTOR FOR GENERATING A NON-INTEGER FREQUENCY DIVISION

ABSTRACT OF THE DISCLOSURE

A frequency divider circuit uses a base counter to frequency divide a clock signal with period T by an integer value N and employs a cyclic rotational select circuit to select among multiple equally phase shifted signals of a multiple phase clock to generate a fractional term P/*k* where P is variable from 0 to *k*-1. The counter counts an output clock that corresponds to the output of a multiplexer selecting from among the multiple clock phases. Depending on the desired fractional term, after N counts of the output clock phases of the multiple phase clock are selected glitch free by rotationally selecting a first phase, and skipping either 0, 1, 2 ... up to *k*-1 sequential phases to generate fractional terms 0, 1/*k*, 2/*k*, 3/*k*...*k*-1/*k*, respectively, thus providing frequency division corresponding to N+P/*k* where P may be varied from 0 to *k*-1.